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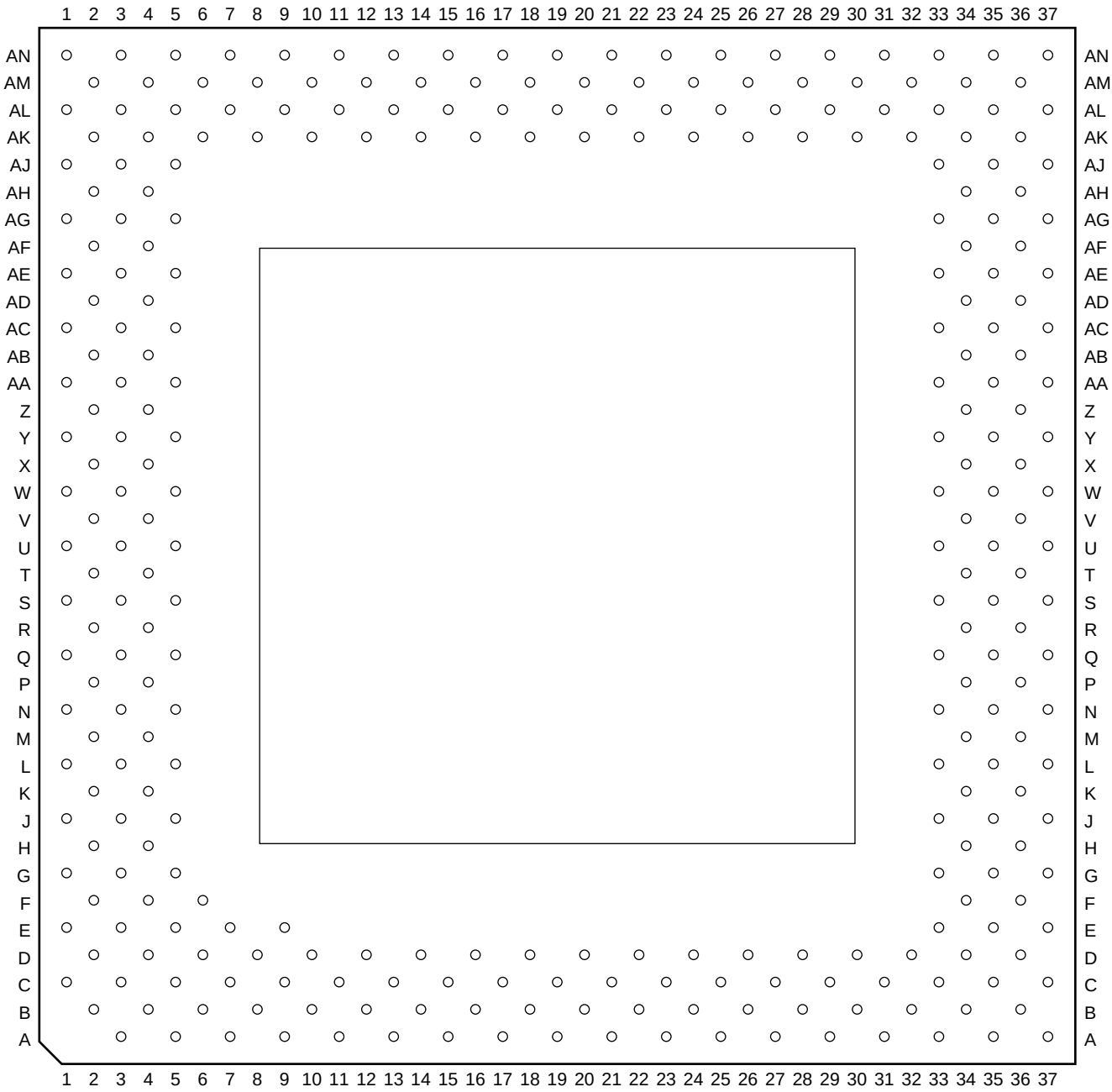
IL22

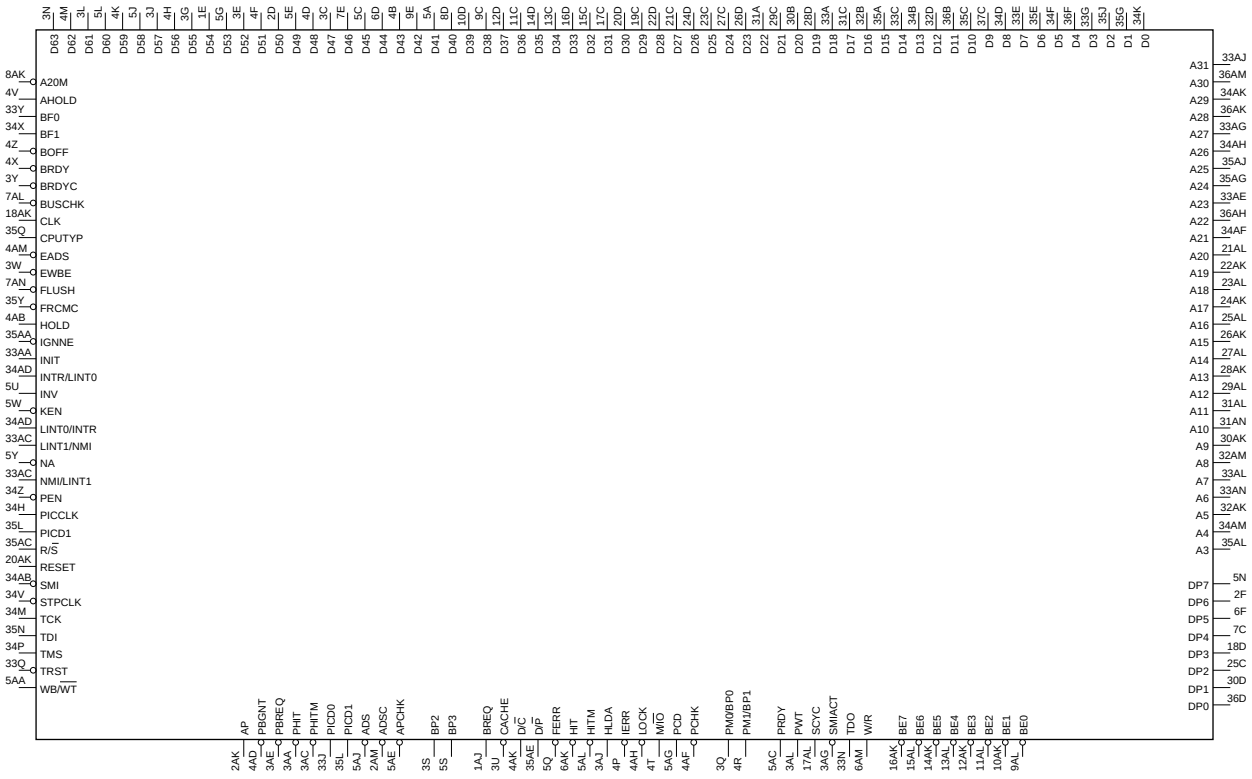
C-MOS 32-BIT CPU WITH 64-BIT DATA BUS

-BOTTOM VIEW-



(V_{DD} = +3.3V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1C	—	INC	4M	I/O	D62	12D	I/O	D37	27C	I/O	D24	35A	I/O	D15
1E	I/O	D54	4P	O	IERR	12AK	I/O	BE3	27AL	I/O	A14	35C	I/O	D10
1G	—	V_{DD}	4R	O	PM1/BP1	12AM	—	GND	27AN	—	V_{DD}	35E	I/O	D6
1J	—	V_{DD}	4T	O	M/IO	13A	—	V_{DD}	28B	—	GND	35G	I/O	D1
1L	—	V_{DD}	4V	I	AHOLD	13C	I/O	D34	28D	I/O	D19	35J	I/O	D2
1N	—	V_{DD}	4X	I	BRDY	13AL	I/O	BE4	28AK	I/O	A13	35L	I/O	PICD1
1Q	—	V_{DD}	4Z	I	BOFF	13AN	—	V_{DD}	28AM	—	GND	35N	I	TDI
1S	—	V_{DD}	4AB	I	HOLD	14B	—	GND	29A	—	V_{DD}	35Q	I	CPUTYP
1U	—	V_{DD}	4AD	I/O	PBGNT	14D	I/O	D35	29C	I/O	D21	35S	—	NC
1W	—	V_{DD}	4AF	O	PCHK	14AK	O	BE5	29AL	I/O	A12	35U	—	GND
1Y	—	V_{DD}	4AH	O	LOCK	14AM	—	GND	29AN	—	V_{DD}	35W	—	NC
1AA	—	V_{DD}	4AK	O	D/C	15A	—	V_{DD}	30B	I/O	D20	35Y	I	FRCMC
1AC	—	V_{DD}	4AM	I	EADS	15C	I/O	D32	30D	I/O	DP1	35AA	I	IGNNE
1AE	—	V_{DD}	5A	I/O	D41	15AL	O	BE6	30AK	I/O	A9	35AC	I	R/S
1AG	—	V_{DD}	5C	I/O	D45	15AN	—	V_{DD}	30AM	—	GND	35AE	O	D/P
1AJ	O	BREQ	5E	I/O	D49	16B	—	GND	31A	I/O	D22	35AG	I/O	A24
1AL	—	INC	5G	I/O	D53	16D	I/O	D33	31C	I/O	D17	35AJ	I/O	A25
1AN	—	INC	5J	I/O	D58	16AK	O	BE7	31AL	I/O	A11	35AL	I/O	A3
2B	—	INC	5L	I/O	D60	16AM	—	GND	31AN	I/O	A10	35AN	—	NC
2D	I/O	D50	5N	I/O	DP7	17A	—	V_{DD}	32B	I/O	D16	36B	I/O	D11
2F	I/O	DP6	5Q	O	FERR	17C	I/O	D31	32D	I/O	D12	36D	I/O	DP0
2H	—	GND	5S	O	BP3	17AL	O	SCYC	32AK	I/O	A5	36F	I/O	D4
2K	—	GND	5U	I	INV	17AN	—	V_{DD}	32AM	I/O	A8	36H	—	GND
2M	—	GND	5W	I	KEN	18B	—	GND	33A	I/O	D18	36K	—	GND
2P	—	GND	5Y	I	NA	18D	I/O	DP3	33C	I/O	D14	36M	—	GND
2R	—	GND	5AA	I	WB/WT	18AK	I	CLK	33E	I/O	D7	36P	—	GND
2T	—	GND	5AC	O	PRDY	18AM	—	GND	33G	I/O	D3	36R	—	GND
2V	—	GND	5AE	O	APCHK	19A	—	V_{DD}	33J	I/O	PICD0	36T	—	GND
2X	—	GND	5AG	O	PCD	19C	I/O	D29	33L	—	V_{DD}	36V	—	GND
2Z	—	GND	5AJ	O	ADS	19AL	—	NC	33N	O	TDO	36X	—	GND
2AB	—	GND	5AL	O	HITM	19AN	—	V_{DD}	33Q	I	TRST	36Z	—	GND
2AD	—	GND	5AN	—	INC	20B	—	GND	33S	—	NC	36AB	—	GND
2AF	—	GND	6B	—	GND	20D	I/O	D30	33U	—	V_{DD}	36AD	—	GND
2AH	—	GND	6D	I/O	D44	20AK	I	RESET	33W	—	NC	36AF	—	GND
2AK	I/O	AP	6F	I/O	DP5	20AM	—	GND	33Y	I	BF0	36AH	I/O	A22
2AM	O	ADSC	6AK	O	HIT	21A	—	V_{DD}	33AA	I	INIT	36AK	I/O	A28
3A	—	INC	6AM	O	W/R	21C	I/O	D27	33AC	I	NMI/LINT1	36AM	I/O	A30
3C	I/O	D47	7A	—	V_{DD}	21AL	I/O	A20	33AE	I/O	A23	37A	—	NC
3E	I/O	D52	7C	I/O	DP4	21AN	—	V_{DD}	33AG	I/O	A27	37C	I/O	D9
3G	I/O	D55	7E	I/O	D46	22B	—	GND	33AJ	I/O	A31	37E	—	V_{DD}
3J	I/O	D57	7AL	I	BUSCHK	22D	I/O	D28	33AL	I/O	A7	37G	—	V_{DD}
3L	I/O	D61	7AN	I	FLUSH	22AK	I/O	A19	33AN	I/O	A6	37J	—	V_{DD}
3N	I/O	D63	8B	—	GND	22AM	—	GND	34B	I/O	D13	37L	—	V_{DD}
3Q	O	PM0/BP0	8D	I/O	D40	23A	—	V_{DD}	34D	I/O	D8	37N	—	V_{DD}
3S	O	BP2	8AK	I	A20M	23C	I/O	D25	34F	I/O	D5	37Q	—	V_{DD}
3U	O	CACHE	8AM	—	GND	23AL	I/O	A18	34H	I	PICCLK	37S	—	V_{DD}
3W	I	EWBE	9A	—	V_{DD}	23AN	—	V_{DD}	34K	I/O	D0	37U	—	V_{DD}
3Y	I	BRDYC	9C	I/O	D38	24B	—	GND	34M	I	TCK	37W	—	V_{DD}
3AA	I/O	PHIT	9E	I/O	D42	24D	I/O	D26	34P	I	TMS	37Y	—	V_{DD}
3AC	I/O	PHITM	9AL	I/O	BE0	24AK	I/O	A17	34R	—	NC	37AA	—	V_{DD}
3AE	I/O	PBREQ	9AN	—	V_{DD}	24AM	—	GND	34T	—	V_{DD}	37AC	—	V_{DD}
3AG	O	SMIACT	10B	—	GND	25A	—	V_{DD}	34V	I	STPCLK	37AE	—	V_{DD}
3AJ	O	HLDA	10D	I/O	D39	25C	I/O	DP2	34X	I	BF	37AG	—	V_{DD}
3AL	O	PWT	10AK	I/O	BE1	25AL	I/O	A16	34Z	I	PEN	37AJ	—	GND
3AN	—	INC	10AM	—	GND	25AN	—	V_{DD}	34AB	I	SMI	37AL	—	GND
4B	I/O	D43	11A	—	V_{DD}	26B	—	GND	34AD	I	INTR/LINT0	37AN	—	GND
4D	I/O	D48	11C	I/O	D36	26D	I/O	D23	34AF	I/O	A21			
4F	I/O	D51	11AL	I/O	BE2	26AK	I/O	A15	34AH	I/O	A26			
4H	I/O	D56	11AN	—	V_{DD}	26AM	—	GND	34AK	I/O	A29			
4K	I/O	D59	12B	—	GND	27A	—	V_{DD}	34AM	I/O	A4			


3N D63
4M D62
3L D61
5L D60
4K D59
5J D58
3J D57
4H D56
3G D55
1E D54
5G D53
3E D52
4F D51
2D D50
5E D49
4D D48
3C D47
7E D46
5C D45
6D D44
4B D43
9E D42
5A D41
8D D40
10D D39
9C D38
12D D37
11C D36
14D D35
13C D34
16D D33
15C D32
17C D31
20D D30
19C D29
22D D28
21C D27
24D D26
23C D25
27C D24
26D D23
31A D22
29C D21
30B D20
28D D19
33A D18
31C D17
32B D16
35A D15
33C D14
34B D13
32D D12
38B D11
35C D10
37C D9
34D D8
33E D7
35E D6
34F D5
36F D4
33G D3
35J D2
35G D1
34K D0
8AK A20M
4V AHOLD
33Y BF0
34X BF1
4Z BOFF
4X BRDY
3Y BRDYC
7AL BUSCHK
18AK CLK
35Q CPUTYP
4AM EADS
3W EWBE
7AN FLUSH
35Y FRCMC
4AB HOLD
35AA IGNNE
33AA INIT
34AD INTR/LINT0
5U INV
5W KEN
34AD LINT0/INTR
33AC LINT1/NMI
5Y NA
33AC NMI/LINT1
34Z PEN
34H PICCLK
35L PICD1
35AC R/S
20AK RESET
34AB SMI
34V STPCLK
34M TCK
35N TDI
34P TMS
33Q TRST
5AA WB/WT
A31 33AJ
A30 36AM
A29 34AK
A28 36AK
A27 33AG
A26 34AH
A25 35AJ
A24 35AG
A23 33AE
A22 36AH
A21 34AF
A20 21AL
A19 22AK
A18 23AL
A17 24AK
A16 25AL
A15 26AK
A14 27AL
A13 28AK
A12 29AL
A11 31AL
A10 31AN
A9 30AK
A8 32AM
A7 33AL
A6 33AN
A5 32AK
A4 34AM
A3 35AL
DP7 5N
DP6 2F
DP5 6F
DP4 7C
DP3 18D
DP2 25C
DP1 30D
DP0 36D
AP 2AK
PBGNT 4AD
PBREQ 3AE
PHIT 3AA
PHITM 3AC
PICD0 33J
PICD1 35L
ADS 5AJ
ADSC 2AM
APCHK 5AE
BP2 3S
BP3 5S
BREQ 1AJ
CACHE 3U
D/C 4AK
D/P 35AE
FERR 5Q
HIT 6AK
HTM 5AL
HLDA 3AJ
IERR 4P
LOCK 4AH
M/IO 4T
PCD 5AG
PCHK 4AF
PM0/BP0 3Q
PM1/BP1 4R
PRDY 5AC
PWT 3AL
SCYC 17AL
SMIACT 3AG
TDO 33N
W/R 6AM
BE7 16AK
BE6 15AL
BE5 14AK
BE4 13AL
BE3 12AK
BE2 11AL
BE1 10AK
BE0 9AL

INPUT

$\overline{A20M}$	;	ADDRESS BIT 20 MASK
AHOLD	;	ADDRESS HOLD
BF0, BF1	;	BUS FREQUENCY
$\overline{BOFF}$	;	BACKOFF
$\overline{BRDY}$	;	BURST READY
$\overline{BRDYC}$	;	THIS SIGNAL HAS THE SAME FUNCTIONALITY AS $\overline{BRDY}$
$\overline{BUSCHK}$	;	BUS CHECK
CLK	;	CLOCK
CPUTYP	;	CPU TYPE
$\overline{EADS}$	;	EXTERNAL ADDRESS
$\overline{EWBE}$	;	EXTERNAL WRITE BUFFER EMPTY
$\overline{FLUSH}$	;	CACHE FLUSH
$\overline{FRCMC}$	;	FUNCTIONAL REDUNDANCY CHECKING MASTER/CHECKER
HOLD	;	BUS HOLD REQUEST
$\overline{IGNNE}$	;	IGNORE NUMERIC ERROR
INIT	;	INITIALIZATION
INTR/LINT0	;	MASKABLE INTERRUPT
INV	;	INVALIDATION
$\overline{KEN}$	;	CACHE ENABLE
LINT0/INTR	;	LOCAL INTERRUPT 0/INTERRUPT
LINT1/NMI	;	LOCAL INTERRUPT 1/NON-MASKABLE INTERRUPT
$\overline{NA}$	;	NEXT ADDRESS
NMI/LINT1	;	NON-MASKABLE INTERRUPT/LOCAL INTERRUPT 1
$\overline{PEN}$	;	PARITY ENABLE
PICCLK	;	PROGRAMMABLE INTERRUPT CONTROLLER CLOCK
PICD1	;	PROGRAMMABLE INTERRUPT CONTROLLER DATA
R/$\overline{S}$	;	RUN/STOP
RESET	;	RESET
$\overline{SMI}$	;	SYSTEM MANAGEMENT INTERRUPT
$\overline{STPCLK}$	;	STOP CLOCK
TCK	;	TESTABILITY CLOCK
TDI	;	TEST DATA
TMS	;	TEST MODE SELECT
$\overline{TRST}$	;	TEST RESET
WB/$\overline{WT}$	;	WRITE BACK/WRITE THROUGH

INPUT/OUTPUT

A3-A31	;	ADDRESS
AP	;	ADDRESS PARITY
$\overline{BE0}$-$\overline{BE4}$	;	BYTE ENABLE
D0-D63	;	DATA LINES
DP0-DP7	;	DATA PARITY
$\overline{PBGNT}$	;	PRIVATE BUS GRANT
$\overline{PBREQ}$	;	PRIVATE BUS REQUEST
$\overline{PHIT}$	;	PRIVATE HIT
$\overline{PHITM}$	;	PRIVATE MODIFIED HIT
PICD0, PICD1	;	PROGRAMMABLE CONTROLLER DATA LINES

OUTPUT

$\overline{ADS}$	;	ADDRESS STATUS
$\overline{ADSC}$	;	$\overline{ADSC}$ IS FUNCTIONALLY IDENTICAL TO $\overline{ADS}$
$\overline{APCHK}$	;	ADDRESS PARITY CHECK
$\overline{BE5}$-$\overline{BE7}$	;	BYTE ENABLE
BP2, BP3	;	BREAKPOINT
$\overline{BREQ}$	;	BUS REQUEST
$\overline{CACHE}$	;	CACHE
D/$\overline{C}$	;	DATA/CODE
D/$\overline{P}$	;	DUAL/PRIMARY
$\overline{FERR}$	;	FLOATING POINT ERROR
$\overline{HIT}$	;	HIT
$\overline{HITM}$	;	HIT TO A MODIFIED LINE
HLDA	;	BUS HOLD ACKNOWLEDGE
$\overline{IERR}$	;	INTERNAL ERROR
$\overline{LOCK}$	;	BUS LOCK
M/$\overline{IO}$	;	MEMORY/INPUT-OUTPUT
$\overline{PCD}$	;	PAGE CACHE DISABLE
$\overline{PCHK}$	;	PARITY CHECK
PM0/BP0, PM1/BP1	;	PERFORMANCE MONITORING/BREAKPOINT
PRDY	;	PROBE READY
PWT	;	PAGE WRITE THROUGH
$\overline{SCYC}$	;	SPLIT CYCLE
$\overline{SMIACT}$	;	SYSTEM MANAGEMENT INTERRUPT ACTIVE
TDO	;	TEST DATA
W/$\overline{R}$	;	WRITE/READ